Fast All-Digital Clock Frequency Adaptation Circuit for Voltage Droop Tolerance

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Abstract :

High-frequency droops in power supply of clocked VLSI circuits are a major component of safety-margins for clock speeds. Clock frequency adaptation circuits try to eliminate these conservative margins by adapting the clock frequency to environmental conditions. The talk presents a highly-reactive clock frequency adaptation design that is based on a new approach of computing with values that are not yet stable.

The talk is based on work with Attila Kinali,
Christoph Lenzen, and Ben Wiederhake.

Minibio :

Matthias Fuegger (http://www.lsv.fr/~mfuegger) received his M.Sc. (2006) and PhD (2010) in computer engineering from TU Wien. He worked as an assistant professor at TU Wien and as a post-doctoral researcher at LIX, Ecole polytechnique (France) and Max-Planck-Institut fuer Informatik (Germany). Currently, he is a CNRS researcher at LSV, ENS Paris-Saclay. His main research interest is the formal study of the fundamentals of computationally restricted distributed devices such as fault-tolerant distributed algorithms in hardware and microbiological systems.